Express Mail No. EV 829 953 566 US

CET-026995
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Doljack et al.	Art Unit:	2831
Serial No.:	10/781,571	Examiner:	Ha, Nguyn T.
Filed:	February 17, 2004		
For:	ACTIVE BALANCING MODULAR CIRCUITS		

DECLARATION OF PRIOR INVENTION

(37 C.F.R. § 1.131)

Hon. Assistant Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Frank Anthony Doljack, whose address is 750 Montevino Dr., Pleasanton, California declares as follows:

1. This declaration is to establish actual reduction to practice of the invention claimed in the above-referenced application at a date prior to April 25, 2003.

2. I have reviewed and understand the patent application referenced in the caption above (hereinafter the "Subject Application"), including the specification, abstract, drawings and claims therefor.

3. I am an inventor of the invention described and claimed in the Subject Application.

4. I have reviewed United States Patent No. 6,806,686 filed on April 25, 2003 (hereinafter the "Antedated Reference"), which has been relied upon to reject at least one claim of the Subject Application.

5. The invention claimed in the Subject Application was reduced to practice before April 25, 2003 which is the filing date of the Antedated Reference.

6. As evidence that the invention was reduced to practice before the filing date of the Antedated Reference, attached hereto as Appendix A is a true and accurate copy of a computer screen shot taken from a computer having a directory of files related to development of the invention.

7. As shown in Appendix A, the directory includes a number of files in a subdirectory labeled "Balancing" that pertain to the development of the invention, and one of the files in the Balancing subdirectory is named "Unitcell1.bmp".

8. I created the file named "Unitcell1.bmp".

9. Attached hereto as Appendix B is a true and accurate printout of the Unitcell1.bmp file. As seen from Appendix B, the file includes a circuit schematic of capacitors connected in series, with active balancing elements connected to the capacitors.

10. More specifically, the drawing of the Unitcell1.bmp illustrates a circuit module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement. The module includes a first terminal configured for connection to a positive plate of the first capacitor; a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor; and a third terminal configured for connection to a negative plate of the second capacitor. An active element is integrated within the inductor-free circuitry between the first, second, and third

terminals and is adapted to substantially balance the voltage imbalances between the pair of capacitors. The active element has power connections to the first and third terminals.

11. Attached hereto as Appendix C is a true and accurate screen shot taken the computer showing the Properties of the Unitcell1.bmp file. As seen in Appendix C, the Unitcell1.bmp file was created on January 13, 2003.

12. As further evidence that the claimed invention was reduced to practice before the filing date of the Antedated Reference, attached hereto as Appendix D are true and accurate copies of documents, including circuit schematics and notes relating to construction and testing of models or prototypes of the invention that were actually constructed.

13. As seen in Appendix D, a working model or prototype of the invention was constructed on February 27, 2003 and was tested on the same day. Further embodiments of the invention were also constructed and tested at various times and dates between March 3, 2003 and March 20, 2003 as Appendix D demonstrates.

14. In Appendix D, handwritten notes are my own and the notes were made as of the date indicated in the documents.

15. As is evident from Appendix D, the constructed embodiments of the invention actually worked for their intended purpose to balance voltages across capacitors connected in series.

16. As still further evidence of a reduction to practice of the invention, attached hereto as Appendix E are drawings (both computer generated and hand sketches) of printed circuit board artwork, and information pertaining to components for the active balancing element used to construct models and/or prototypes of the invention at a date prior to April 25, 2003.

17. The computer generated drawings include footers indicating the dates that the drawings were printed. As seen from Appendix E, all of the computer drawings were printed at a date prior to April 25, 2003.

18. All activities documented in the factual evidence of Appendices A through E occurred in the United States.

19. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Frank Anthony Doljack Jun 16, 2006

Frank Anthony Doljack **(Date)**